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Design of Low Power and Power Scalable Pipelined ADC Using Current Modulated Power Scale-A Review

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Abstract: *A set of low-power techniques proposed to realize low power design in pipeline analogue-to-digital converter (ADC). These techniques include removing the active S/H (i.e., SHA-less), sharing the opamp between the adjacent multi-bit-per-stages, low-power high-efficiency high-swing amplifier technique. Also, a new sampling topology proposed to minimize aperture error by matching the time constant between the two input signal paths. This paper presents an in-depth review of a 10-bit pipelined Analog to Digital Converter (ADC) which incorporates various techniques for lesser power and higher performance.*

Keywords: Successive Approximation Register, Low power, Resolution, Sampling Rate.

1. Introduction

A 10-bit pipelined Analog to Digital converter (ADC) designed such that its average power is scalable with a sampling rate over a considerable variation of sampling rates. The ADC uses a fast power resettable Opamp (PROamp), to achieve power scalability between sampling rates as high as 50 Msps, as low as 1ksps while having 54-56 dB of SNDR for all sampling rates.

Since analog subsystems are carefully characterized and optimized by setting specific bias currents, a significant variation of bias currents to reduce power with speed, furthermore, as bias currents reduced, transistors shift from strong to weak inversion operation.

Low-power analog-to-digital converters (ADCs) with 10– 12-bit resolution and several tens of MHz sampling rates recognized as one of the significant components in portable or battery-operated commercial applications including data communication and image signal processing systems. Recently, a lot of low-power technologies are proposed and verified in several designs. However, the time-interleaving architecture easily limited by offset and gain mismatches as well as aperture errors between the interleaved channels [1].

The performance of the pseudo-differential architecture [2] compared with that of the fully differential one, is sensitive to the common-mode voltage and substrate or power supply noise. Complex calibration schemes and circuit techniques [3], which are usually needed to enhance the linearity and correct the mismatches such as compensating low gain, low bandwidth and incomplete settling of opamps, need a complicated algorithm, additional digital circuitry and extra calibration cycles. SHA-less and opamp-sharing are two important ways for low-power pipelined ADC design [4]. However, they also bring some drawbacks affecting the ADC performance, such as nonlinearity and distortion. How to tradeoff and get rid of these harmful factors are the hot points in the low-power Pipelined ADC design area. Reference [5] makes use of dummy sampling capacitances and complicated digital calibration without opamp-sharing to enhance the SNR and SFDR performance. The proposed structure in [6] may not be suitable for the ADCs that expected to run at the maximum achievable sampling rate for a given resolution and technology, Because the opamp used in the proposed first stage needs to be faster, simultaneously meaning more power consumption, than the one in the traditional first stage[7].

A current modulation technique used to avoid weakly inverted transistors for low bias currents, thus avoiding less accurate simulation, more unsatisfactory matching, and increased bias sensitivity. The resettable power Opamp used. Simulated results show an ADC using power resettable Op-amp has 30-40% less power than an ADC which does not use resettable power Opamp [8].

In many mixed-signal systems, Analog-to-Digital Converters (ADC) required for interfacing analog signals to digital circuits[9]. Sigma Delta ADC architectures are very useful for lower sampling rate and higher resolution (approximately 12-24 bits). The common applications for Sigma-delta ADC architecture are found in voice band, audio and industrial measurements. The Successive Approximation (SAR) architecture is very suitable for data acquisition; it has resolutions ranging from 8 bits to 12 bits and sampling rates ranging from 50 kHz to 50 MHz. The most effective way to create a Giga rate application with 8 to 16-bit resolution is the pipeline ADC architecture. Here in this, we are presenting SAR ADC because, in the past few years, more and more applications built with very stringent requirements on power consumption.

2. ADC architecture

The main power dissipation of the pipeline ADC comes from amplifiers. The power dissipation could be cut

down by more than 50 per cent by reduction of the number of amplifiers through the amplifier-sharing and SHA-less technology compared with the standard architecture with S/H [10]. The proposed ADC architecture is shown in Figure 1.

There are five stages in the ADC. Each of the first four stages is 2.5-bit per step and generates two significant bits, and the last flash ADC gives three effective bits. There are only two active opamps utilized in the ADC. The first opamp shared by the first SHA-less stage and the second stage, and the second opamp shared by the third and the fourth stages. Each flash ADC in the first four stages consists of 6 low power dynamic comparators, and the last flash ADC built up with seven comparators. The clock generator, digital correction logic and current-to-voltage bias voltage generation circuit also included in the ADC.

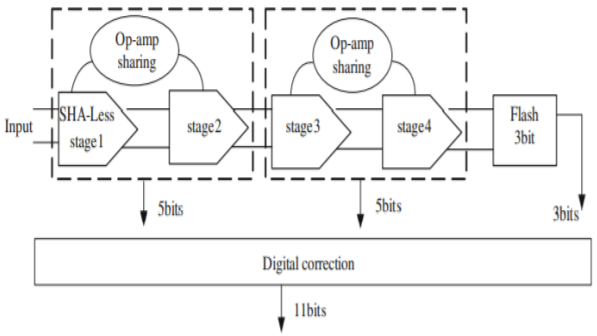

Figure 1: Architecture of ADC

3. RELATED WORK

3.1 Literature Review of 10-Bit ADCS

A brief review of publication on 10-bit presented here. As a discussion of the approaches used in each publication would be prohibitively long, this section takes note of the key performance metrics for this work, namely power, accuracy and speed.

An increasing number of IC compatible sensors demand suitable readout circuits with on-chip ADC to reduce the signal sensitivity to perturbations on the circuit and at the sensor interface, decrease system complexity and cost, as well as enable further on-chip digital processing like data correction. Applications like wireless sensor nodes and medical diagnose always require at least 12-bit linearity and noise performance and extremely low power consumption (as low as 100μW) because of the battery operation. Besides, to meet the requirements of large sensor arrays, the ADC must occupy a small silicon area and can be multiplexed between multiple channels. A 100μW, 13bit ADC used for sensor array applications is presented in paper [1].

A pipelined analog-to-digital converter (ADC) architecture suitable for high-speed (150 MHz), Nyquist-rate A/D conversion presented. At the input of the converter, two parallel track-and-hold circuits used to separately drive the sub-ADC of a 2.8-b first pipeline stage and the input to two time-interleaved residue generation paths. Beyond the first pipeline stage, each residue path includes a cascade of two 1.5-b pipeline stages followed by a 4-b "backend" folding ADC. The full-scale residue range at the output of the pipeline stages is half that of the converter input range to conserve power in the operational amplifiers used in each residue path. An experimental prototype of the proposed ADC has been integrated into a 0.18-/spl mu/m CMOS technology and operates from a 1.8-V supply. At a sampling rate of 150 MSample/s, it achieves a peak SNDR of 45.4 dB for an input frequency of 80 MHz. The power dissipation is 71 mW[2].

Article[3] describes a 10-bit 30-MS/s subsampling pipelined analog-to-digital converter (ADC) that implemented in a 0.18 mum CMOS process. The ADC adopts a power-efficient amplifier sharing architecture in which additional switches introduced to reduce the crosstalk between the two opamp-sharing successive stages. A new configuration is used in the first stage of the ADC to avoid using a dedicated sample-and-hold amplifier (SHA) circuit at the input and to avoid the matching requirement between the first multiplying digital-to-analog converter (MDAC) and flash input signal paths.

Article[4] describes a 12-bit 125-MS/s pipelined analog-to-digital converter (ADC) that implemented in a 0.18 μm CMOS process. A gate-bootstrapping switch is used as the bottom-sampling switch in the first stage to enhance the sampling linearity. The measured differential and integral nonlinearities of the prototype are less than 0.79 least significant bit (LSB) and 0.86 LSB, respectively, at the full sampling rate.

Complex calibration schemes or circuit techniques [5], which are usually needed to enhance the linearity and correct the mismatches such as compensating low gain, low bandwidth and incomplete settling of opamps, need a complicated algorithm, additional digital circuitry and extra calibration cycles.

The residue amplifiers in high-speed pipelined analog-to-digital converters (ADCs) typically determine the converter's overall speed and power performance. We propose a mixed-signal technique that exploits incomplete settling to achieve low power residue amplification. In the first stage of a 12-bit, 75-MS/s proof-of-concept prototype, the employed open-loop residue amplifier dissipates only 2.9 mW from a 3-V supply, achieving >60% amplifier power reduction over

a previously reported open-loop residue amplifier implementation and achieving >90% amplifier power reduction over a conventional opamp implementation [6].

This work covers the device and circuit aspects of low-power analog CMOS circuit design. The fundamental limits constraining the design of low-power circuits first recalled with an emphasis on the implications of supply voltage reduction. Biasing MOS transistors at shallow current provide new features but require dedicated models valid in all regions of operation including weak, moderate and strong inversion. Low-current biasing also has a strong influence on noise and matching properties. All these issues are discussed, together with the particular aspects related to passive devices and parasitic effects. The design process has to be supported by an efficient and accurate circuit simulation. To this end, the EKV compact MOST model for circuit simulation is presented [7].

A 10-b 20-Msample/s analog-to-digital converter fabricated in a 0.9- mu m CMOS technology described. The converter uses a pipelined nine-stage architecture with fully differential analog circuits. It achieves a signal-to-noise-and-distortion ratio (SNDR) of 60 dB with a full-scale sinusoidal input at 5 MHz[8].

A 10 bit 60 MS/s Low-Power Pipelined ADC with Split-Capacitor CDS Technique. The proposed pipelined ADC fabricated in a pure digital 0.18-µm CMOS process consumes 18 mW at 60 MS/s from a 1.8 V power supply, without power scalability [9].

Authors of [10] proposed a 10 bit 30-Msps sub-sampling pipelined ADC that implemented in a 0.18 m CMOS process. The ADC consumes 21.6mW from a 1.8 V power supply.

Seung-Tak Ryu et al., uses power and area-saving concepts such as operational amplifier (Op-amp) bias current reuse and capacitive level shifting for a 10-bit pipelined ADC. The prototype achieves 8.8 effective numbers of bits (ENOB) for 50 MS/s. The ADC consumes 28 mW at 1.8V [11].

Masato Yoshioka et al., given a 10 bit, 125Msps, CMOS pipelined analog to digital converter. The power consumption of this ADC is 40mW at a supply voltage of 1.8V and SNDR is 54.2 dB[12].

Article [13] given a 10 bit, 100Msps, CMOS pipelined ADC using time-shifted CDS technique. The power consumption of this ADC is 67mW at a supply voltage of 1.8V and SNDR is 54 dB.

D. Miyazaki et al., the proposed design of 10 bit 30 MS/s low-power CMOS ADC described. The ADC using a pseudo-differential architecture and a capacitor cross-coupled sample-and-hold stage consumes 16 mW with a single 2V supply [14].

A 10 bit, 25Msps, CMOS pipelined ADC using a low-voltage Op-amp-reset switching technique. The power consumption of this ADC is 21mW at a supply voltage of 1.4V and SNDR is 48 dB [15].

3.2 SURVEY OF POWER SCALABLE ADCS

To date power, scalable ADCs have not been an active area of research, and as such, there are very few publications which target a scalable power over a large range of sampling rates [16]. All published reports of ADCs with scalable power use bias current scaling to reduce power with sampling rate. In industry, however, several 10-bit ADCs have been developed which have a scalable power.

High-speed architectures (f_s-max>10Msps) achieve lower power for lower sampling rates using current scaling. They are shown in datasheets to have a small power scalable range (<1:100), likely due to poorer yield at lower sampling rates as transistors driven into weak inversion. Low-speed architectures (<500ksps) achieve power scalability by powering off the ADC between conversion samples[17]. Due to the slow power on/off times of ADCs however, the technique of powering off an ADC between conversions is limited to slower architectures, based on a survey of commercial 10-bit power scalable ADCs. A study of power scalable ADCs in the industry given in Table 1.1.

Table 1.1 Survey of Power Scalable ADCs in Industry

No.	Company	Model	Speed (Msps)	Power (mW)	SNDR	P.Scaling method*
1	ADI	7467	0.05	0.48	61	A
2	ADI	7811	0.01	0.315	58	A
3	ADI	7811	0.1	3.15	58	A
4	ADI	7811	0.35	10.5	58	A
5	ADI	9203	40	75	59.3	B
6	Maxim	Max1086	0.05	0.1755	61	A
7	Maxim	Max1086	0.15	0.54	61	A
8	Nordic VLSI	nAD1050-18	10	8	59	B
9	Nordic VLSI	nAD1050-18	50	33	59	B
10	Fairchild Semi	SPT7883	50	105	60	B

*A is when ADC is Power off between conversion
*B is when current scaling used to reduce power with a sampling rate

4. Conclusions

Several feasible low-power techniques, including removing the active S/H (SHA-less) with a new sampling topology, sharing the opamp between the adjacent multi-bit-per-stages, low-power high-efficiency high-swing amplifier technique, are proposed by many research articles. In this article, try to review the multiple ADC/DAC designs are implemented in different technologies to address either high-speed or low-power

design challenges or even both. Circuit design techniques and considerations extensively and carefully discussed in both architectural and transistor level.

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