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# Analysis and Design of a 2D DCT Transform Using Angle Recorded CORDIC Algorithm

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***Abstract -*** *Digital signal processing (DSP) algorithms show an accumulative essential for the efficient implementation of complex arithmetic processes. The computation of trigonometric functions, coordinate transformations, or rotations of complex-valued phasors is nearly naturally convoluted with modern DSP algorithms. In this paper, one of the furthermost computationally high algorithms called the Discrete Cosine Transform is implemented with the help of CORDIC(Coordinate Rotation Digital computer) algorithm, which results in a multiplier fewer architectures and assessment is made among the DCT using Chen's algorithm and DCT using CORDIC as well as novel CORDIC algorithm.*

***Keywords:- PID Controller, user datagram protocol, network control system, dc servo motor, Smith predictor.***

## 1. INTRODUCTION

DCT is usually used transform in image processing, exclusively for compression. Particular applications of two-dimensional DCT include still image compression and compression of different video frames, although multidimensional DCT is typically recycled for compression of video streams and volume spaces. Transform is also convenient for transferring multidimensional data to the DCT frequency domain, where altered operations, similar spread-spectrum data watermarking, can be completed in an easier and additional efficient way. An uncountable number of papers deliberating DCT algorithms are sturdily perceiving its status and applicability. Hardware executions are particularly exciting for realizing highly parallel algorithms that accomplish far higher than software solutions. In addition, distinct resolve DCT hardware discharges the computational load from the processor and thus develops the performance of the whole multimedia system. The quantity is directly manipulating the quality of experience of multimedia content. An additional significant factor that affects the quality is the finite register length consequence on the accuracy of the forward-inverse transformation process. Discrete cosine transform (DCT) is widely used in image processing, particularly for compression. Some applications have two DCT sizes for still image compression and single frame compression, and many DCT sizes are often used for video stream compression. DCT and useful for transferring multidimensional data to the frequency domain, where various operations such as spectrum propagation, data compression, and data watermarking can be performed more simply and efficiently. Several articles discuss DCT algorithms available in the literature, and hence their meaning and application.

## 2. LITERATURE SURVEY

This paper's principal reference is reference [4] titled "Low-power Multiplier less DCT architecture using Image Data Correlation." The AR CORDIC algorithm is brought from that reference and, of course, later modified. Those modifications are in reducing the number of iterations and scaling factor. Later the main idea about CORDIC is from references [3, 5, 6, 7, 8]. Those references are correctly described CORDIC. Later the VLSI implementations and architectures are in reference [9, 17, 19], where Yu Hen Hu correctly described the different architectures of CORDIC in VLSI, and FU also described the architectures. Later the different implementations of DCT in VLSI are given in reference [11], which is a tutorial like this. Before that, all the references about DCT 3 are given in reference [16, 21], where they briefly understand DCT. Later the design of another important block in the design of DCT Core, i.e., Transpose buffer, is given in reference [12]. The VHDL tutorial is given from reference [1, 2], which gives a good understanding of VHDL.

## 3. PROBLEM STATEMENT

Discrete cosine transform is one of the most transformative technologies in digital signal processing. In addition, it is also the most computationally intensive turning, which requires a large number of multiplications and additions. Real-time data processing requires special equipment, which means that computer equipment is characterized by efficiency and high throughput. Many DCT algorithms offer to achieve high-speed DCT. The architecture represents a multiplier; for example, the mode B algorithm has a small low-end architecture, routing difficulties, and requires a large silicon area; on the other hand, DCT- based distributed architectures count (A) in an architecture that is speed-free, have inherent drawbacks not in bandwidth, but rather such as time availability and battery need. In addition, this algorithm requires that on a large area of silicon, even though it requires large ROM sizes. The systolic array architecture for real-time DCT calculation can have many ports and clock skew problems.

## 4. PROPOSED ALGORITHM

Over the past decade, thanks to major advances in VLSI technology, modeling has generated a great deal of interest in developing special parallel processor arrays to facilitate digital signal processing in real-time. Parallel processor arrays are systolic arrays that have been extensively studied. The basic calculation is like parallel VLSI arrays, often using Unified multiplication and accumulation (MAC) because these actions often occur in a DSP program. Reducing hardware costs and motivation is to develop advanced DSP algorithms that require evaluation of basic functions such as trigonometric, exponential, and logarithmic functions that can be efficiently evaluated using MAC-based unit counting. Therefore, when DSP algorithms include elementary functions, there is often a significant performance penalty.

## 5. RESULT AND ANALYSIS

It is better to keep the accuracy-we took a narrow width of 45. So, the error is 1%, which can be easily ignored. So, with the CORDIC algorithm, we can compensate for it, low power, and compact design even if it is an error. These results are often displayed in data results. Now consider the DCT design of the CORDIC algorithm. Then, design at a high level to keep accurate. We need a little bit of width. For example, when calculating 3pi / 8, the maximum value of I will be 13, which means that we have good accuracy, the information must be at least 50 bits wide, so large IOBs are automatically required and, in turn, a large area. Subsequently, we used DCT images and PSNR comparison of three-dimensional slides created by DCT algorithm mode in which DCT help, "CORDIC algorithm," and then DCT using the New Cordic algorithm." Now let's go to view the free report that is generated by Xilinx ISE 9.1.

Table 1: Simulation Results

| Algorithm used | Area | Power Consumption (Xpower) |
|---|---|---|
| Conventional Chen's algorithm | 6.76% of total resources | 261.43 MW is the peak power consumption |
| Angle recoded CORDIC | 4.62% of total resources | 210.20 MW of peak power consumption |
| The New CORDIC algorithm | 5.67% of total resources | 222.50 MW of peak power consumption |

For the families that are used, it is synthesized below. The synthesis results show that the DCT mode input algorithm takes up much space, which consumes much electricity since this factor is the existing algorithm, DCT CORDIC algorithm, and the lower angle under code Cordic algorithm in terms of area and energy consumption. In addition, there must be a trade-off between the required precision and the input bit width. For example, to get the exact precision of 4 decimal places after the decimal point, the input bit width is 43 bits was wider than 48 bits, not that this is a very large part of the width, which is the basis for the CORDIC algorithm codes. The requirements for high accuracy and the smaller surface area, smaller power, and the angle of the encoded DYNAMIC algorithm- the fate of all the final reports are given in the form of a table.

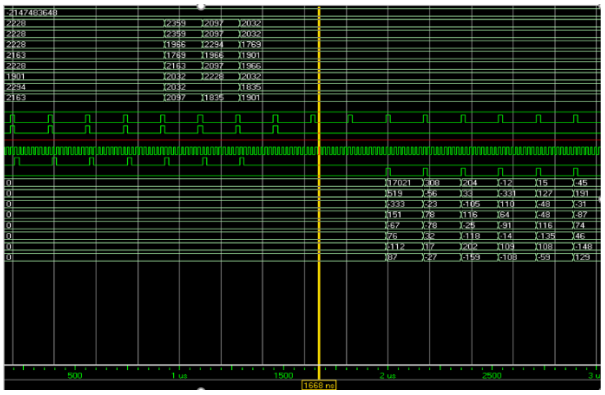

Figure 1 Timing Diagram shows the DCT results using the New CORDIC algorithm.

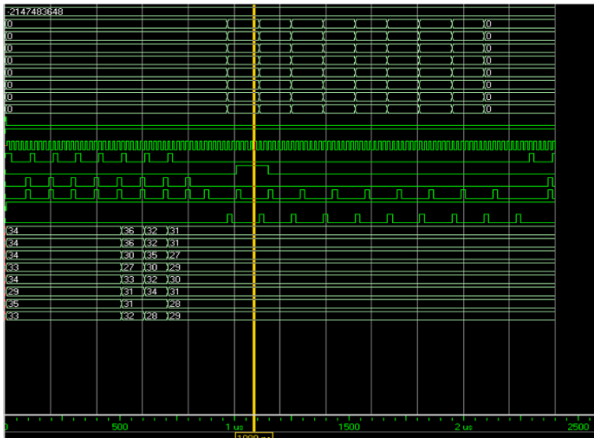

Figure 2 Timing diagram showing the DCT results using AR CORDIC algorithm

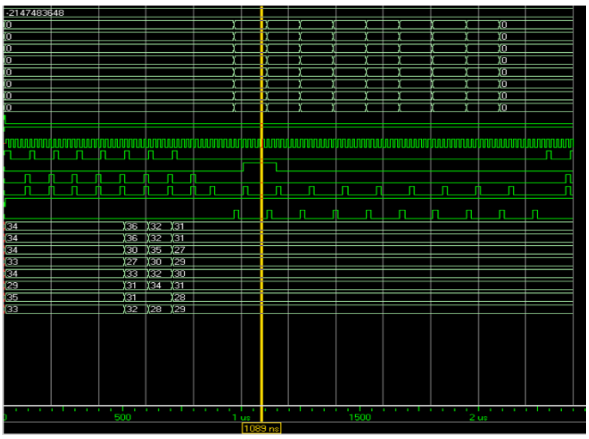

Figure 3 Timing diagram showing the DCT results using the New CORDIC algorithm

## 6. CONCLUSION AND FUTURE SCOPE

Digital signal processing (DSP) algorithms provide countries with an increasing need for efficient and efficient implementation of complex arithmetic operations. Calculations of trigonometric functions, changes, or rotations of complex-valued phasors, we can say that, of course, modern-sounding algorithms work—a well-known example of the application of algorithms used in digital communication technologies and adaptive signal processing. It is important to estimate the features listed above in digital communication, and many matrix-based adaptive signal processing algorithms require solving systems of linear equations, QR factorization, or counting their values, direction, or singular values. All these tasks can be implemented using a processing element that performs vector rotation. The Digital Coordinate Rotation Computing Algorithm (CORDIC) offers the ability to calculate all the features you want in a very simple and elegant way. DCT, based on the CORDIC algorithm, does not need a multiplier. In addition, permanent core and simple hardware are available, making it easy to implement in VLSI. In addition, the CORDIC-based DCT algorithm can support high program performance, including HDTV-based streaming of CORDIC algorithm for higher-order DCT systems DCT computation and simulation for more points implementation and simulation for DHT and DST calculations.

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